IN THE CLAIMS:

Please amend the claims as follows:

Claim 1 (Currently Amended): A method for compressing a set of instructions for a node in a adaptive computing machine, the method comprising:

identifying frequently executed instruction in the set of instructions for an information processing device;

inserting an explicit caching instruction in the set of instructions before the identified instruction, wherein the explicit caching instruction associates the identified instruction with at least one index value, the at least one index value referencing an area of an instruction storage unit; and

replacing at least one instance of the frequently executed instruction subsequent to the explicit caching instruction with a compressed instruction referencing the at least one index value, wherein the compressed instruction directs an information processing device to execute the identified instruction associated with the at least one index value wherein the frequently executed instruction is accessible from the instruction storage unit using the at least one index value.

Claim 2 (Previously Presented): The method of Claim 1, wherein the step of identifying includes identifying a subset from the set of instructions comprising a plurality of instructions.

Claim 3 (Previously Presented): The method of Claim 2, wherein the subset comprises a plurality of consecutive instructions from the set of instructions.

Claim 4 (Previously Presented): The method of Claim 2, wherein the explicit caching instruction directs an information processing device to store the subset of instructions in an instruction storage unit in association with the at least one index value.

Claim 5 (Previously Presented): The method of Claim 4, wherein the instruction storage unite has a storage element associated with the at least one index value, such that the subset of instructions stored in the storage element can be retrieved with reference to the at least one index value.

Claim 6 (Previously Presented): The method of Claim 4, wherein the instruction storage unit has a plurality of storage elements, each storage element associated with an index value, and the explicit caching instruction directs an information processing device to store each instruction of the subset of instructions in one of the plurality of storage elements, such that each one of the instructions can be retrieved with reference to the index value associated with the storage element.

Claim 7 (Previously Presented): The method of Claim 2, wherein the subset of instructions is part of an inner loop.

Claim 8 (Previously Presented): The method of Claim 1, wherein the explicit caching instruction directs a node in an adaptive computing machine to store the identified instruction in the instruction storage unit in association with the at least one index value.

Claim 9 (Previously Presented): The method of Claim 8, wherein the instruction storage unit has a storage element associated with the at least one index value, such that the instruction stored in the storage element can be retrieved with reference to the at least one index value.

Claim 10 (Cancelled)

Claim 11 (Previously Presented): The method of Claim 6 wherein the compressed instruction includes a plurality of references to the index values, each reference to the index values directing an information processing device to execute the instruction stored in the storage element associated with the referenced index value.

Claim 12 (Previously Presented): The method of Claim 11 wherein the plurality of references to the index values are arranged in a sequence indicating the sequence of execution of the associated instructions.

Claim 13 (Previously Presented): A method for executing a set of instructions for an information processing device, the method comprising:

retrieving a primary instruction within the set of instructions from a memory;

when the primary instruction is an explicit caching instruction, storing at least one instruction subsequent to the primary instruction in an instruction storage unit; and

when the primary instruction is a compressed instruction, retrieving, from the instruction storage unite, the at least one previously stored instruction using the compressed instruction and executing the at least one previously stored instruction.

Claim 14 (Previously Presented): The method of Claim 13, wherein the explicit caching instruction stores a subset comprising a plurality of instructions from the set of instructions.

Claim 15 (Previously Presented): The method of Claim 14, wherein the explicit caching instruction sores a subset comprising a plurality of consecutive instructions from the set of instructions.

Claim 16 (Previously Presented): The method of Claim 14, wherein the explicit caching instruction stores the subset of instructions in association with at least one index value.

Claim 17 (Previously Presented): The method of Claim 16, wherein the explicit caching instruction stores each of the subset of instructions in one of a plurality of storage elements, each storage element associated with an index value, such that each one of the instructions can be retrieved with reference to the at least one index value associated with the storage element.

Claim 18 (Previously Presented): The method of Claim 13, wherein the explicit caching instruction stores the at least one instruction in association with an index value.

Claim 19 (Previously Presented): The method of Claim 18, wherein the compressed instruction includes the index value for retrieving and executing the at least one instruction associated with the index value.

Claim 20 (Previously Presented): An adaptive computing machine configured to compress a set of instructions for a node, wherein the adaptive computing machine comprises one or more processors and a memory containing logic that, when processed by the one or more processors, cause the one or more processors to perform a set of steps comprising:

identifying frequently executed instruction in the set of instructions for an information processing device;

inserting an explicit caching instruction in the set of instructions before the identified instruction, wherein the explicit caching instruction associates the identified instruction with at least one index value, the at least on index value referencing an area of an instruction storage unit; and

replacing at least one instance of the frequently executed instruction subsequent to the explicit caching instruction with a compressed instruction referencing the at least on index value, wherein the frequently executed instruction is accessible from the instruction storage unit using the at least one index value.